This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,211	09/26/2001	Nicholas G. Samra	42390.P8999	2932

7590 06/30/2004

Maria McCormack Sobrino
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,211	SAMRA ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-16,19,21-29* is/are rejected.

7)☒ Claim(s) *7,8,17,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6,9-16,19,21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Zaidi (patent No. 6,065,105)(submitted by applicant).

2. Zaidi taught the invention as claimed including a data processing ("DP") system comprising:

a) Dependency matching logic (dependency determination unit and dependency matrix) to receive a first dependency coordinate corresponding to a dependency relationship, the dependency matching logic upon receiving the first and second dependency coordinates, to identify whether the first dependency precludes scheduling (e.g., see figs. 2,3 and col. 4, line 1-col. 6, line 49); and

b) Dependency checking logic (Ready logic and Zero detection logic) to produce a ready signal if the dependency matching logic has not identified that scheduling was precluded (e.g., see col. 5, lines 58-64 and col. 6, line 61-col. 7, line 4).

3. As per claims 2,3,10,11,13,19,21,22 Zaidi taught separate dependency coordinates or vectors in the dependency matrix for each instruction stored in the waiting buffer therefore comprised dependency vector corresponding to the first location

in the waiting buffer and each dependency vector corresponded to the waiting buffer (e.g., see col. 5, lines 13-41).

4. As per claim 4. Zaidi taught the buffer that the dependency vector corresponded comprised a functional buffer arrangement (e.g., see col. 5, lines 13-41).

5. As per claim 5,15 Zaidi taught a scheduling information interface (32)(e.g., see col. 4, line 54-col. 5, lines 41).

6. As per claims 6, 16, The memory of Zaidi taught a means to enable writing of data into the memory (e.g., see fig. 5 and col. 8, lines 9-34).

7. As per claim 9,14,21 Zaidi taught means for generating first and second dependency vectors (e.g., see fig. 5), dispatching the first instruction and using the first instruction coordinate to access the second dependency coordinate in response to the first instruction being dispatched and dispatching a second instruction (e.g., see col. 8, line 9-col. 9, line 43).

8. As per claim 12,21 Zaidi taught the system implementing in a microprocessor (e.g, see col. 1, lines 6-9). Consequently it would have been required for the system to access machine accessible (namely microprocessor accessible) medium to program the microprocessor such a memory.

9. As to the limitations of claim 23,24 Zaidi taught an instruction fetcher. Also since the Zaidi system comprised a microprocessor it would have been required to decode instruction when high level instructions were used program the system (e.g, see col. 1, lines 6-9).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi (patent No. 6,065,105).

12. Zaidi taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Dependency matching logic (dependency determination unit and dependency matrix) to receive a first dependency coordinate corresponding to a dependency relationship, the dependency matching logic upon receiving the first and second dependency coordinates, to identify whether the first dependency precludes scheduling (e.g., see figs. 2,3 and col. 4, line 1-col. 6, line 49); and

b) Dependency checking logic (Ready logic and Zero detection logic) to produce a ready signal if the dependency matching logic has not identified that scheduling was precluded (e.g., see col. 5, lines 58-64 and col. 6, line 61-col. 7, line 4).

13. As per claims 2,3,10,11,13,19,21,22 Zaidi taught separate dependency coordinates or vectors in the dependency matrix for each instruction stored in the waiting buffer therefore comprised dependency vector corresponding to the first location in the waiting buffer and each dependency vector corresponded to the waiting buffer (e.g., see col. 5, lines 13-41).

14. As per claim 4. Zaidi taught the buffer that the dependency vector corresponded comprised a functional buffer arrangement (e.g., see col. 5, lines 13-41).

15. As per claim 5,15 Zaidi taught a scheduling information interface (32)(e.g., see col. 4, line 54-col. 5, lines 41).

16. As per claims 6, 16, Zaidi taught a means to enable writing of data into the memory (e.g., see fig. 5 and col. 8, lines 9-34).

17. As per claims 9,14,21 Zaidi taught means for generating first and second dependency vectors (e.g., see fig. 5), dispatching the first instruction and using the first instruction coordinate to access the second dependency coordinate in response to the first instruction being dispatched and dispatching a second instruction (e.g., see col. 8, line 9-col. 9, line 43).

18. As per claims 12,21 Zaidi taught the system implemented in a microprocessor (e.g., see col. 1, lines 6-9). Consequently it would have been required for the system to access machine accessible (namely microprocessor accessible) medium to program the microprocessor such a memory.

19. As to the limitations of claim 23,24 Zaidi taught an instruction fetcher. Also, since the Zaidi system comprised a microprocessor it would have been required to decode instruction when high level instructions were used program the system (e.g., see col. 1, lines 6-9).

20. As per claims 25-29, Zaidi did not expressly detail emulated data or emulated instruction, or that the instruction was a micro or macroinstruction. However since the Zaidi system was implemented on a microprocessor and using dependency checking

one of ordinary skill would have been motivated to use standard instructions that comprised macroinstructions that were well known to be decoded into microinstructions for execution. This would have allowed the system for execution the instruction set to be less complicated than if each instruction had to have unique micro-operations as it would have used selected micro-operations from a set of micro-operations. It also would have been easier to program. Also the use of a moderate number of instructions such as in a RISC implementation and emulation of instruction outside the instruction set would have allowed for a faster implementation of instructions within the instruction set using less costly decoding circuitry (e.g., see col. 1, lines 11-65).

21. Claims 7,8,17,18,20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schrader (patent No. 6,366,993) disclosed a dependency controller for overlapping memory access operations (e.g., see abstract).

Scheaffer (patent No. 5,710,902) disclosed an instruction dependency chain idendifier (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER